A VLSI Architecture of a Binary Updown Counter

I. S. Reed
University of Southern California

I. S. Hsu and T. K. Truong
Communications Systems Research Section

In this article, a new pipeline binary updown counter with many bits is developed which can be used in a variety of applications. One such application includes the design of a digital correlator for very long baseline interferometry (VLBI) [1].

The advantage of the presently conceived approach over the previous techniques is that the number of logic operations involved in the design of the new binary updown counter can be reduced substantially. The architecture design using these methods is regular, simple, expandable and, therefore, naturally suitable for VLSI implementation.

I. Introduction

Large binary updown counters are widely used in digital circuits. Examples include the controller design of a servomotor or the correlator part of very long baseline interferometry (VLBI) [1]. In [7], a VLSI design of an up counter is used as a model for an updown counter. In that design, only two one-bit registers and a half adder are needed in each stage and its expansion to implement a counter with more bits is very easy and straight forward. However, a fixed bias value is added to the sum. Therefore, the sum "zero" is represented as the middle value of the range of the numbers and the smallest negative number is represented by "zero". Also, it takes n clock times to perform one counting operation in the worst case.

In this article, a new design of a large pipeline binary updown counter is presented. The design of this new updown counter is simple, regular and expandable. Also, only one clock time is needed to perform one counting operation. Using this new architecture it is verified that a 64-bit binary updown counter can be put readily on a single VLSI chip with current NMOS technology. An example describing the pipeline architecture as well as the simplicity of each basic cell of this new counter is illustrated completely for a 3-bit case.

II. A New Algorithm for a Binary Updown Counter

In this section, a new algorithm is developed for the implementation of a binary updown counter. This algorithm is illustrated by an example for a 3-bit case. However, the same structure clearly can be extended to the more general cases.

Let the input to this counter have three values, namely, -1, 0, and 1. The input is fed into the counter sequentially. Also let $A_n(t)$ denote the value of the nth bit of a clocked counter at time t. Then it can be verified easily by the techniques in [2] that

$$A_n(t) = A_n(t-1) \oplus ((U \cdot P_n) \cup (D \cdot Q_n)) \qquad (1)$$

where there is no loss of generality to assume time t is integer-valued and where $A_n(t-1)$ is the value of the nth bit of an updown counter at time $t-1$. Also in Eq. (1) the symbol "$\oplus$" denotes "exclusive OR" operation. The symbol "$\cdot$" denotes "AND" operation and the symbol "$\cup$" is the "inclusive OR" operation. If $U = 0$ and $D = 1$, then the input is "-1". If both U and D equal zero, then the input is "0". In Eq. (1), P_n represents product of A_k's, for $1 \leqslant k \leqslant n-1$, while Q_n is the product of $\bar{A}_k$'s, for $1 \leqslant k \leqslant n-1$, where $\bar{A}_k$ is the complemented value of A_k. Both P_n and Q_n are expressed as the following two equations:

$$P_n = A_{n-1} A_{n-2} \cdots A_1 \qquad (2\text{-a})$$

$$Q_n = \bar{A}_{n-1} \bar{A}_{n-2} \cdots \bar{A}_1 \qquad (2\text{-b})$$

Equation (2) can be rewritten in a recursive form as

$$P_n = P_{n-1} \cdot A_{n-1} \qquad (3\text{-a})$$

and

$$Q_n = Q_{n-1} \cdot \bar{A}_{n-1} \qquad (3\text{-b})$$

with the initial values $P_1 = 1$ and $Q_1 = 1$. Intuitively, Eq. (1) can be described as follows:

If the input to the counter is a "0", then the contents of the counter should remain unchanged. It is easily verified from Eq. (1) that $A_n(t) = A_n(t-1)$ with $U = D = 0$.

If the input is "0", both U and D equal "0" according to the previous assignments. This will null the second term in Eq. (1) and by the property of "exclusive OR", one yields $A_n(t) = A_n(t-1)$.

On the other hand, if the input is "1", then $U = 1, D = 0$. The second term of Eq. (1) $(U \cdot P_n \cup D \cdot Q_n)$, is then changed to $(1 \cdot P_n) \cup (0 \cdot Q_n) = P_n$. This equals 1 if $P_n = 1$ which implies $A_1 = A_2 = \cdots = A_{n-1}$. In counting up, the value of nth bit changes from zero to one if (1) input to the counter is a "1" and (2) the value of bit 1 to bit $n-1$ are all ones. This fact is truthfully reflected by Eq. (1). A similar argument applies to the case when the input to the counter is a "-1", i.e., the counter is counting down.

III. Example of the New Updown Counter

We illustrate the new algorithm with the design of a 3-bit binary updown counter.

The truth table of a 3-bit binary updown counter is shown in Table 1. Where $A_i(t)$, for $i = 1, 2, 3$, denotes value of ith bit of the counter at time t. To verify this truth table, consider, for illustation the 4th row in Table 1.

In this row,

$$D = 0, \quad U = 1, \quad A_3(t) = 0, \quad A_2(t) = 1, \quad A_1(t) = 1.$$

This corresponds to the case for which the contents of counter is digit 3 in binary and the input is "1". Obviously, the next value should equal four. Namely, $A_3(t+1) = 1$, $A_2(t+1) = 0$ and $A_1(t+1) = 0$.

Substituting these values of A_i, for $i = 1, 2, 3$, as well as the values $U = 1, D = 0$ into Eq. (1), yields the following results:

$$\begin{aligned} A_3(t+1) &= A_3(t) \oplus (U \cdot P_3 \cup D \cdot Q_3) \\ &= 0 \oplus (1 \cdot 1 \cup 0 \cdot 0) \\ &= 0 \oplus 1 \\ &= 1 \end{aligned}$$

In the above substitutions one uses the fact that

$$P_3 = A_1 \cdot A_2 = 1$$

and

$$Q_3 = \bar{A}_1 \cdot \bar{A}_2 = 0.$$

Also,

$$\begin{aligned} A_2(t+1) &= A_2(t) \oplus ((U \cdot P_2) \cup (D \cdot Q_2)) \\ &= 1 \oplus ((1 \cdot 1) \cup (0 \cdot 0)) \\ &= 1 \oplus 1 \\ &= 0 \end{aligned}$$

and

$$A_1(t+1) = A_1(t) \oplus ((U \cdot P_1) \cup (D \cdot Q_1))$$

$$= 1 \oplus ((1 \cdot 1) \cup (0 \cdot 0))$$

$$= 1 \oplus 1$$

$$= 0$$

The rest-states of Table 1 can be verified in a similar manner.

IV. A VLSI Architecture for Implementing an *n*-bit Binary Updown Counter

In this section, a VLSI architecture is developed for an n-bit binary updown counter. This VLSI counter is composed of n basic cells as well as a data mapping programmable logic array (PLA) [3]. The ith basic cell carries out the operations for calculating P_i, Q_i, and A_i.

Figure 1 shows a pipeline architecture for an n-bit binary updown counter. It is composed of n basic cells and a data conversion PLA. Input to the data conversion PLA is either 1, 0 or -1. These three values are represented as 01, 00 and 10 respectively in binary representation. It is true that if the input numbers are represented in accordance with this format, then this PLA is not needed. However, it is required in general to match to the outside system. Output of this PLA are values of U and D. As described in the previous section, if input value is a "1" then $U = 1$ and $D = 0$. If input is a "-1", then $U = 0$ and $D = 1$. Both U and D are zero if input is a "0". In Fig. 2, a block diagram as well as a table illustrate the relationship between the input and output of this PLA.

Inputs to the ith basic cell are U, D, P_i and Q_i while the outputs are U, D, P_{i+1}, Q_{i+1} and A_{i+1}. Outputs P_{i+1} and Q_{i+1} are obtained by the calculation of Eqs. (2a) and (2b). A_{i+1} is the intermediate value of a switch bit of this counter. For an n-bit binary updown counter, n identical basic cells are required in the design.

Figure 3 shows the logic diagram of a basic cell in Fig. 1. This basic cell consists of three one-bit shift registers where registers labeled as RQ_i and RP_i are used to store values of Q_i and P_i respectively. Register RA_i stores value of A_i. The output of RA_i is sent to an XOR circuit for calculating the value of $A_i(t+1)$. In the mean time, A_i together with its complementary value $\overline{A}_i$ is sent to two AND gates for the calculation of P_{i+1} and Q_{i+1}. Figure 4 shows the logic diagram of a one-bit shift register. The two-phase clocking scheme is adopted in this design for the ease of timing control.

As was described previously, the initial values of P_n and Q_n are $P_1 = Q_1 = 1$. Therefore the inputs to registers of the first basic cell RP_1 and RQ_1 are tied to VDD which is always at logic value "one".

Figure 5 shows the pin assignment of an n-bit binary updown counter. Where VDD and GND are power pins, ϕ_1 and ϕ_2 are two inputs for the non-overlapping clocks. A_i, for $1 \leqslant i \leqslant n$ are the output pins representing the results of counting. The final value is obtained n time units after the last input fed into the counter. Figure 6 shows the layout of a 64-bit binary updown counter. This was carried out by using the CAD system described in [8]. The total chip area is approximately 6000 X 5700 μm^2. The area occupied by the counter circuit is only 2800 X 2600 μm^2. The difference is due to the large number of input and output pads needed to interface with the outside world.

V. Conclusion

An efficient architecture has been developed for the VLSI implementation of a binary updown counter. The architecture is easily extensible in the number of bits counted. A 64-bit binary updown counter is designed according to this new algorithm. It is demonstrated in this article that a 64-bit binary updown counter can be realized easily on a single VLSI chip with current NMOS technology.

References

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Table 1. The change of state of a 3-bit binary updown counter and *U* and *D* values

D	U	$A_3(t)$	$A_2(t)$	$A_1(t)$	$A_3(t+1)$	$A_2(t+1)$	$A_1(t+1)$
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	1
0	1	0	1	1	1	0	0
0	1	1	0	0	1	0	1
0	1	1	0	1	1	1	0
0	1	1	1	1	0	0	0
0	1	1	1	0	1	1	1
1	0	0	0	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	0	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0

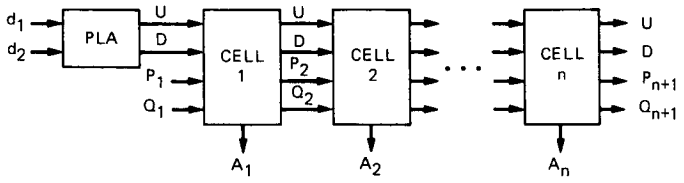
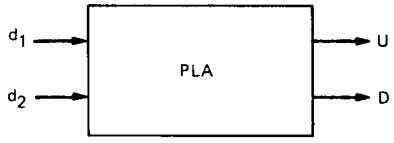


Fig. 1. Pipeline architecture for an *n*-bit binary updown counter



d_1	d_2	U	D
0	0	0	0
0	1	0	1
1	0	1	0

Fig. 2. Block diagram and truth table of a data conversion PLA

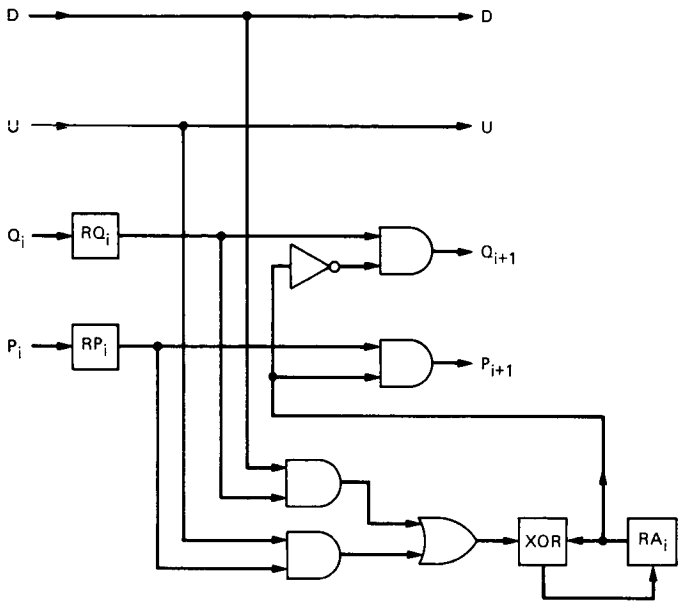


Fig. 3. Logic diagram of a basic cell of an *n*-bit updown counter

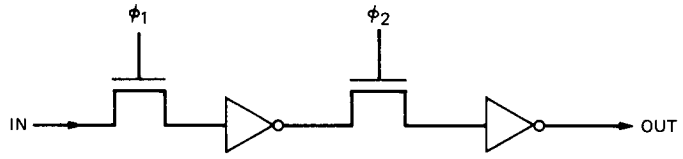


Fig. 4. Logic diagram of a 1-bit shift register

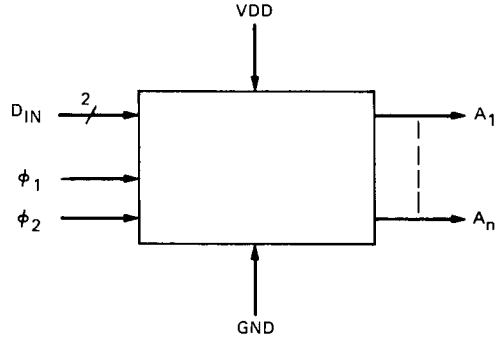


Fig. 5. Pin assignment diagram of an *n*-bit binary updown counter

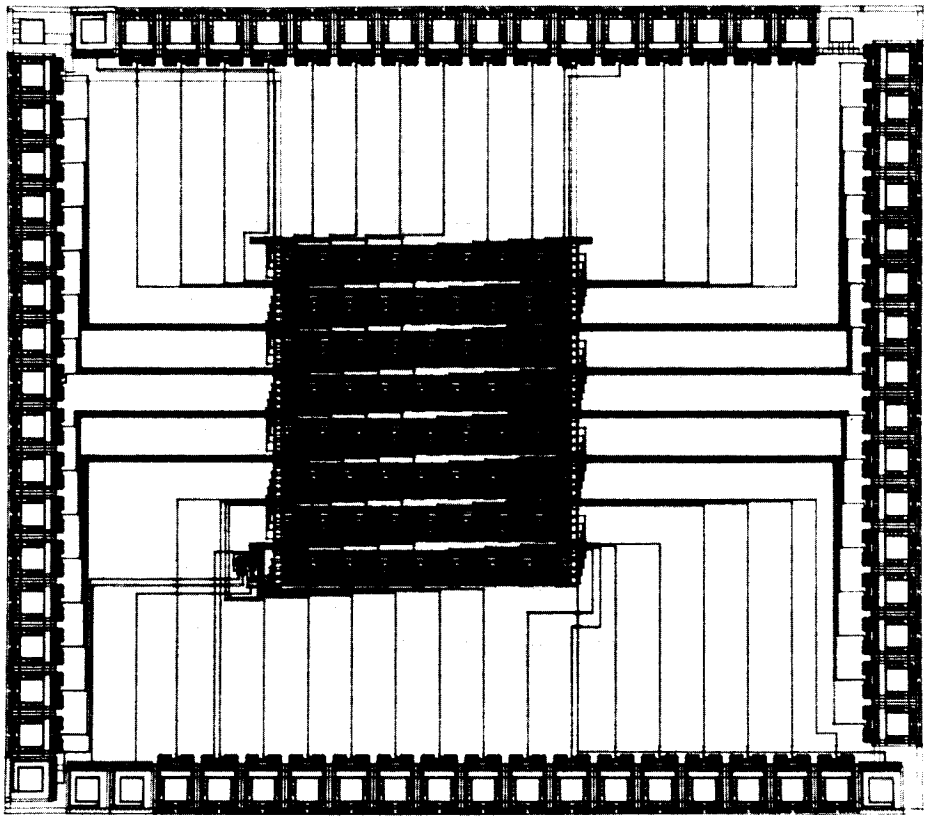


Fig. 6. VLSI layout of a 64-bit updown counter